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TITLE

THIN-FILM TRANSISTOR ARRAY STRUCTURE

BACKGROUND OF THE INVENTION

Field of the invention

This invention relates to a Thin-Film Transistor array structure. More particularly, this invention relates to a Thin-Film Transistor array structure for sustaining all capacitance-coupling effects between a source electrode and a data line of a panel.

Description of Prior Art

For the manufacture of a Thin-Film Transistor (TFT) array of a panel, especially in the case of those with a larger size, the exposure process on the TFT has to be divided and proceeded by several steps.

However, the alignment of the layers between each two adjacent exposed blocks of the TFT is easily dislocated during the exposure process, and the capacitance-coupling effects between a source electrode and a data line on each of the adjacent exposed blocks are very different. Thus, the penetrating rates of each block of the TFT are different in typical TFT structures.

Referring to Fig. 1A, Fig. 1A is a plan view showing the structure of one pixel of typical TFT structure. Symbol "CE" represents a common electrode, symbol "SL" represents a scanning line, symbol "10" represents a TFT, and symbol "DL" represents a data line. The drain electrode 12 of the TFT 10 is coupled to an ITO electrode (i.e. pixel electrode) 16 via a contact hole 14 formed on an isolated layer, and the data line DL is coupled to a

drain electrode 18 of the TFT 10.

Fig. 1B is a cross-section according to a line I-I of Fig. 1A. A distance Δd existing between the data line DL and the ITO electrode 16 is formed during the exposure process and is an important parameter related to the capacitance-coupling effect of two adjacent blocks of the TFT 10. Once the distance Δd exceeds a predetermined value, the capacitance-coupling effect of the adjacent blocks is easily affected and causes a visible line on the panel.

SUMMARY OF THE INVENTION

To solve the above problem, the primary object of this invention is to provide a TFT array structure, which comprises a Thin-Film Transistor, a data line, a scanning line, a pixel electrode and an auxiliary electrode. The data line is connected to the drain of the Thin-Film Transistor, and the scanning line is connected to the gate of the Thin-Film Transistor. The scanning line is oriented substantially orthogonally with respect to the data line to form a plurality of rectangular pixels in matrix. The auxiliary electrode is formed at the place where the pixel electrode is close to the edge of the data line, and the auxiliary electrode is coupled to the pixel electrode and located at a mask on which the data line is located. The capacitance-coupling effect generated between the pixel electrode and the data line is the same as that generated between the predetermined electrode and the data line, and the performances of all pixels are uniform despite errors occurring during the aligning process on the pixel electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by

reading the subsequent detailed description and examples with reference made to accompanying drawings in which:

Fig. 1A is a plan view showing the structure of one pixel of typical TFT structure.

Fig. 1B is a cross-section according to a line I-I of Fig. 1A.

Fig. 2A is a plan view showing the structure of one pixel of a TFT structure according to one embodiment of the present invention.

Fig. 2B is a cross-section according to a line II-II of Fig. 2A.

Fig. 3 is a plan view showing the structure of one pixel of a TFT structure according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 2A is a plan view showing the structure of one pixel of a TFT structure according to one embodiment of the present invention, and Fig. 2B is a cross-section according to a line II-II of Fig. 2A.

The TFT array structure comprises a Thin-Film Transistor 20, a data line 22, a scanning line 24, a pixel electrode 26 and a common electrode CE. The data line 22 is coupled to a drain electrode 20a of the Thin-Film Transistor 20, and the scanning line 24 is coupled to a gate electrode 20b of the Thin-Film Transistor 20 and crossed to the data line 22 to form a plurality of rectangular pixels in matrix. The pixel electrode 26 is constructed at each of the pixels and coupled to a source electrode of the Thin-Film Transistor 20 via a contact hole 28 which is formed on an isolated layer (not shown). A source electrode 20c of the Thin-Film Transistor 20 is extended to the region (both sides of the data line 22)

where the pixel electrode 26 is next to the data line 22, and the edge of the pixel electrode 26 is disposed onto the source electrode 20c.

Fig. 2B is a cross-section according to a sectional line II-II of Fig. 2A. In Fig. 2B, it is understood that the capacitance-coupling effect is mainly generated between the data line 22 and the source electrode 20c. As the source electrode 20c and the data line 22 are formed on the same mask and the pixel electrode 26 is coupled to the source electrode 20c via a contact hole 28, the capacitance-coupling effect generated between the pixel electrode 26 and the data line 22 is the same as that generated between the source electrode 20c and the data line 22. Further, the distance between the source electrode 20c and the data line 22, located at the same mask, is constant, and the edge of the pixel electrode 26 is located above the source electrode 20c and located within the range of the source electrode 20c. Despite the distance between the source electrode 20c and the data line 22 being slightly uneven during the formation of the pixel electrode 26, the capacitance-coupling effect generated between the pixel electrode 26 and the data line 22 remains the same, based on the constant distance between the source electrode 20c and the data line 22.

Fig. 3 is a plan view showing the structure of one pixel of a TFT structure according to another embodiment of the present invention.

The TFT array structure comprises a Thin-Film Transistor 20, a data line 22, a scanning line 24, a pixel electrode 26 and an auxiliary electrode 30. The data line 22 is connected to the drain 20a of the Thin-Film Transistor 20, and the scanning line 24 is connected to the gate 20b of the Thin-Film Transistor 20. The scanning line

24 is oriented substantially orthogonally with respect to the data line 22 to form a plurality of rectangular pixels in matrix. The pixel electrode 26 is constructed at each of the pixels and coupled to a source electrode 21 of the Thin-Film Transistor 20 via a contact hole 28. The auxiliary electrode 30 is extended to the region (both sides of the data line 22) where the pixel electrode 26 is next to the data line 22, and the edge of the pixel electrode 26 is disposed onto the auxiliary electrode 30. The auxiliary electrode 30 is coplanar with the source electrode 21 and coupled to the source electrode 21 of the Thin-Film Transistor 20 via a contact hole 32.

Because the auxiliary electrode 30 is coupled to the source electrode 21 and the pixel electrode 26, the capacitance-coupling effect generated between the pixel electrode 26 and the data line 22 is the same as that generated between the auxiliary electrode 30 and the data line 22. The source electrode 20c and the data line 22 are located at the same mask and the distance between the auxiliary electrode 30 and the data line 22 is constant. Despite the formation of the pixel electrode 26 being uneven, the capacitance-coupling effect generated between the pixel electrode 26 and the data line 22 remains the same, based on the constant distance between the auxiliary electrode 30 and the data line 22.

The above pixel electrode 26 is generally an ITO (Indium Tin Oxide) electrode, and the material for forming the auxiliary electrode 30 is the same as the material for forming the source electrode 21. The source electrode 20c in the first embodiment is formed in a U-shaped structure, and the auxiliary electrode 30 in the second embodiment is formed in an H-shaped structure. It is characterized that a predetermined electrode (source electrode 20c or

auxiliary electrode 30) is formed at the place where the pixel electrode is close to the edge of the data line. The predetermined electrode is coupled to the pixel electrode and located at a mask on which the data line is located. It is also characterized that the capacitance-coupling effect generated between the pixel electrode and the data line is the same as that generated between the predetermined electrode and the data line. The performances of all pixels are uniform despite errors occurring during the aligning process on the pixel electrode.

While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.